ABSTRACT OF THE DISCLOSURE

In one embodiment of the present invention, a bus controller is used in a multi-bus system having first and second buses. The bus controller includes first and second bus interface circuits, a processor interface circuit, and an arbitration logic circuit. The first and second bus interface circuits interface to the first and second buses, respectively. The first bus is accessible to a first processor. The processor interface circuit interfaces to a second processor. The arbitration logic circuit is coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors.